

5.8 Dual-Port CMOS Image Sensor with Regression-Based HDR Flux-to-Digital Conversion and 80ns Rapid-Update Pixel-Wise Exposure Coding

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Today's best consumer cameras typically use computational imaging techniques to digitally enhance images by means of software post-processing to yield both high fidelity and low cost. A common technique, for example, is to combine multiple shots with different camera settings into one enhanced image that has a high dynamic range (HDR). This post-processing-based approach fails when fast motion and/or rapidly changing illumination are present, as often happens in autonomous driving, drone imaging, and action-camera applications, or when the illumination itself is actively controlled (e.g., for depth sensing). These applications require a much tighter temporal integration of: (1) in-pixel processing, (2) pixel readout, and (3) post-capture enhancement. Aiming to address these needs, a new class of 'coded' computational image sensors has emerged, with both fine (i.e., per-pixel) [1-3] and coarse (i.e., per-pixel-cluster) [4] programmable exposure control. Some of these sensors offer spatial exposure control for single-shot HDR imaging [1,2], but require multiple ADC types and/or a number of pre- and post-processing steps (e.g., adaptive pixel-wise exposure control, HDR reconstruction, etc.). Other coded sensors support a variety of computational imaging techniques (e.g., robust depth imaging, compressed sensing [3]), but their conventional ADCs do not offer HDR readout. HDR sensors exist that digitize the pixel output during exposure, before it saturates, but offer no coding [5,6].

We introduce an image sensor with an ADC-free flux-readout scheme that can output one or more digital HDR flux samples per frame, based on sinusoidal-reference comparator binary outputs that are read out at 26kHz during exposure. Our readout scheme, which we call Regression-based Flux-to-Digital Conversion (RFDC), offers wider dynamic range compared to conventional ADC architectures, is generally applicable to any (non-SPAD) pixel design and reduces digital processing to a simple pixel-wise regression. A second contribution of our image sensor is the support for 80ns rapid-update pixel-wise exposure coding at rates more than two orders of magnitude faster than the state of the art. This functionality enables capture of light with fast-changing intensity, and is independent and complementary to our RFDC scheme.

While single-slope (SS) ADC is the architecture of choice in most CMOS image sensors (CIS), mainly due to its compactness and linearity, it typically offers limited dynamic range, speed and energy efficiency. The SS-ADC consists of a comparator and a shared global ramp generator. As shown in Fig. 5.8.1 (top, left), the voltage corresponding to the integrated photogenerated charge is sampled at the end of the exposure period and compared by the SS-ADC with a ramped reference voltage. The timestamp of the comparator output transient is then converted to a digital number corresponding to the pixel intensity. However, the pixel's full-well-capacity (FWC) limits the sensor's dynamic range for high flux, and its output is only available at the end of the exposure. Our programmable-rate RFDC scheme, on the other hand, estimates light flux while the pixel is being exposed, as illustrated in Fig. 5.8.1. RFDC uses only a comparator with a sinusoidal reference voltage. In the simplest version of our scheme (Fig. 5.8.1 (top, right)), the timestamp of the comparator output transient is used to estimate the instantaneous incident flux (flux is equal to the line's slope). High flux values simply trigger the comparator earlier in the exposure period, before the pixel saturates. This allows for capturing scenes with a wider dynamic range. As RFDC operates during the exposure, no extra readout time is required.

A sinusoidal waveform serves as a good approximation for the theoretically derived HDR-optimum shape of the reference voltage. As opposed to a ramp or other time-varying waveforms employed with SS-ADCs, a low-noise sinusoidal voltage can be generated using negligibly small power. We take advantage of this fact by using a multi-period sinusoidal reference voltage to further boost the signal-to-noise ratio (SNR) of the measured flux. Figure 5.8.1 (bottom, left) shows that such an approach yields multiple comparator output transients within one exposure period, which can then be used to improve the flux estimations by line fitting. Lower-flux pixels cross the sinusoidal reference voltage the maximum number of times (four times in the example shown), and higher-flux pixels cross at least once. For line fitting, we use linear regression as it also reduces the effect of the reset noise (corresponding to the offset of the fitted line) and acts as a viable alternative to the conventional correlated-double-sampling (CDS) technique. Extending this further, one can increase the number of sinusoidal cycles to enable piecewise-linear fitting and detect multiple flux values before resetting the pixel, as shown in Fig. 5.8.1 (bottom, right). This potentially allows for estimating motion in the scene within a single frame, as long as the pixel does not saturate.

In addition to its RFDC readout scheme, the image sensor enables rapid pixel-wise coding, which allows for capturing light with fast-changing intensity. Figure 5.8.2 (left) depicts a block diagram of the image sensor, which has two respective ports: (1) fast per-pixel-exposure binary code inputs at the maximum rate of 12.5M pixel rows per second, with each port addressable by an independent random-access row decoder, and (2) comparator outputs at the maximum effective rate of 26k binary pixel array readouts per second used to estimate intra-frame HDR flux. As opposed to [1,2,4] where spatially coded exposure control is fully used up to enable HDR imaging, in this sensor the HDR is offered by the RFDC, freeing up the per-pixel coded-exposure control functionality for other computational imaging applications.

Up to 870 full-frame comparisons can be performed at 30fps with the IC consuming only 8.56mW. The linear regression adds a very small power overhead – it requires computing an inner product of two low-dimensional vectors (e.g., three-five dimensions in Fig. 5.8.1 (bottom)).

Pixel-wise exposure coding is implemented using a two-tap pixel design inspired by the indirect time-of-flight (iToF) pixel, but with two key differentiators: (1) iToF pixel performs fixed temporal coding only (Fig. 5.8.2 (right, top)), whereas our pixel includes per-pixel charge-sorting circuitry between taps 1 and 2, which enables pixel-wise spatial exposure programmability, and (2) a moderate charge transfer contrast of 60-70% is sufficient for iToF pixel as it operates on phase measurements, whereas our pixel enables applications that have much stricter contrast requirements, above 90-95%; this limits the coded subexposure rate to around 12.5MHz versus higher operating iToF frequencies. Also, many reported spatially coded computational image sensors offer coarse-resolution coding on pixel clusters (Fig. 5.8.2 (right, second from top)), for example on a 16x16 pixel grid [4], effectively reducing the coded-sensor spatial resolution by a large factor (e.g., by 256x in [4]). Our pixel performs coding at the native spatial resolution (Fig. 5.8.2, right, third from top) and scales well to stacked-wafer technologies by means of local temporal multiplexing on small pixel groups, without the need for large 3D interconnect in each pixel or large temporal lag. Finally, our coded subexposure rate is a factor of up to 320x higher than the fastest previous pixel-wise exposure coding implementation [1], owing to the random-access nature of the code update port (Fig. 5.8.2, right, fourth from top), and to the fact that many coded imaging techniques require sparse temporal code updates (e.g., only in a single row or a few rows at a time). To facilitate fast and low-power code delivery, as shown in Fig. 5.8.2 (left, top), a custom code generator can locally generate three types of common codes without having to spend the power to ship them from off the chip.

Figure 5.8.3 depicts the circuit diagrams of the pixel and readout path, and the corresponding timing diagrams. The processes of pixel coding and RFDC can be temporally staggered or interleaved, offering an extra degree of freedom for various computational imaging techniques.

Figure 5.8.4 illustrates the experimentally measured RFDC SNR and the pixel charge-transfer contrast. A total dynamic range of 95dB has been measured, with SNR ranging between approximately 10 and 42dB, for four VREF-VIN crossings per RFDC output.

Figure 5.8.5 shows the raw experimentally measured output and reconstructed HDR image mapped by log-compression to a low-dynamic-range (LDR) space using a four-comparison RFDC. The RFDC output is split into four images to show the outputs at the four different VREF-VIN crossings, one per VREF half-period during the exposure.

Figure 5.8.6 depicts the comparative analysis table. Figure 5.8.7 shows the micrograph of the image sensor fabricated in a 110nm CIS process. The 3.67mW flux-to-digital converter bank has a very small foot-print and was used to obtain all experimental results.

References:

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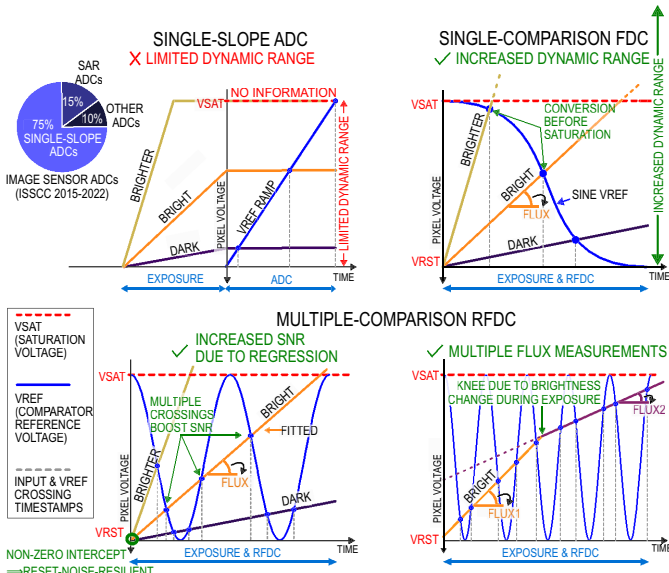


Figure 5.8.1: SS-ADC vs regression-based flux-to-digital converter (RFDC) with single and multiple comparisons.

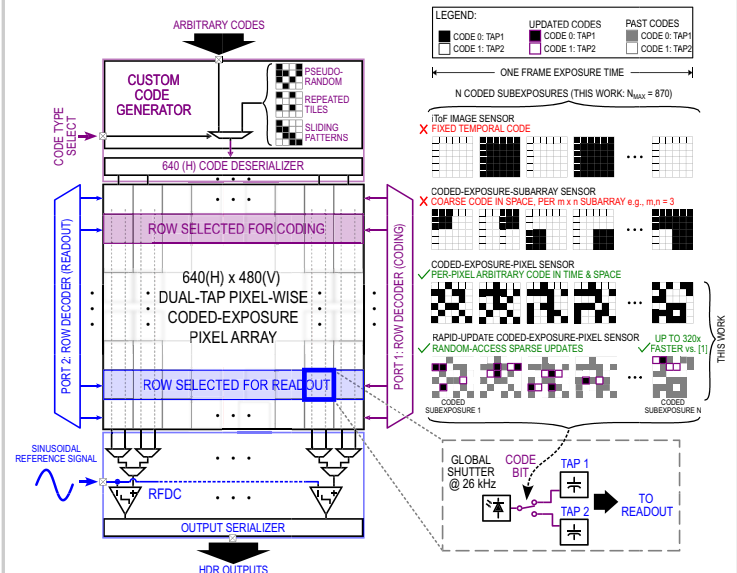


Figure 5.8.2: Image sensor block diagram and various coding strategies that are implemented on the chip.

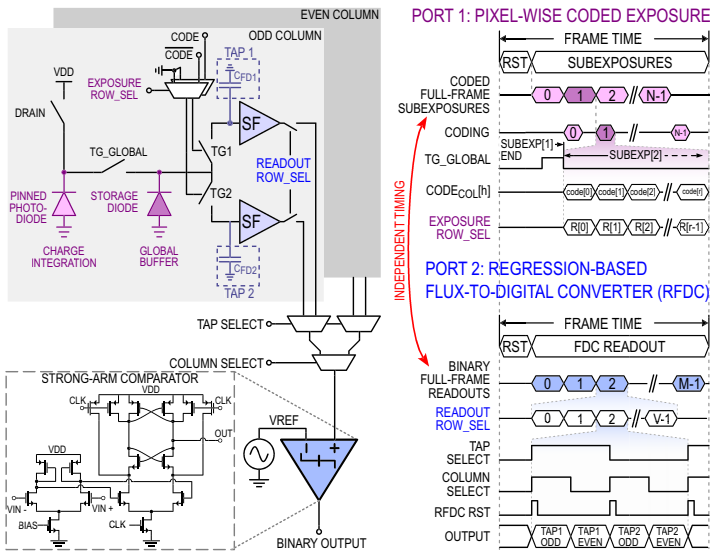


Figure 5.8.3: Coded-exposure pixel, regression-based flux-to-digital converter (RFDC), and their timing diagrams.

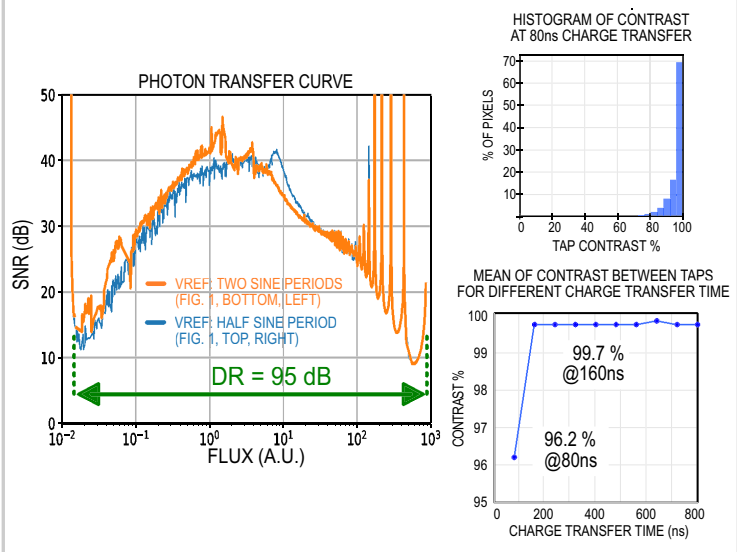


Figure 5.8.4: Experimentally measured photon transfer curve and contrast characterization.

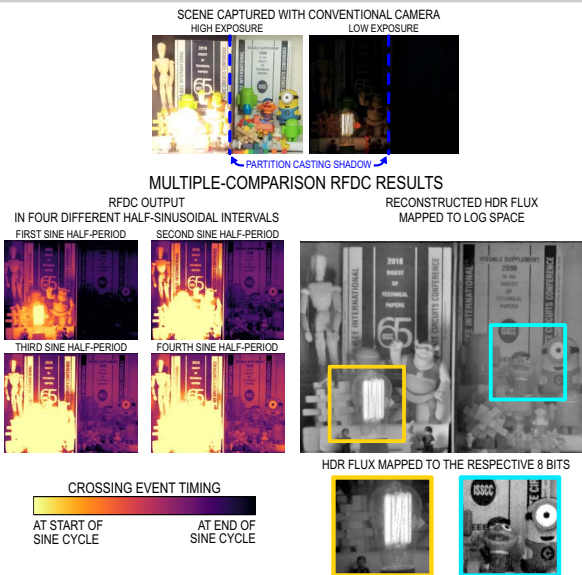


Figure 5.8.5: Experimentally measured results with reconstructed HDR image using multiple-comparison RFDC.

	THIS WORK	[6] Yonsei ISSCC 2022	[1] Toronto VLSI 2022	[5] META TED 2022	[3] UBC JSSC 2022	[2] Canon ISSCC 2022	[4] Nikon ISSCC 2021
SYSTEM							
TECHNOLOGY [nm]	110 CIS	250 CMOS	110 CIS/ 65 CMOS	45 CIS/ 65 CMOS	130 CIS	90 SPAD/ 40 CMOS	65 CIS/ 65 CMOS
PIXEL PITCH [μm]	7 (PPD)	10 (PG)	7 (PPD)	4.6 (PPD)	12.6 (PG)	11.1 (SPAD)	2.7 (PPD)
RESOLUTION	640x480	120x120	320x320	512x512	192x192	960x960	4200x4200
FRAME SHUTTER	GLOBAL	ROLLING	GLOBAL	GLOBAL	GLOBAL	GLOBAL	GLOBAL
POWER [mW]	8.56	0.0132	122	5.75	31.5	330	--
POWER FoM [pJ/frame-pixel]	929	22.9	10700	731	28030	3978	--
HDR READOUT							
FLUX-TO-DIGITAL CONVERTER	FULL RANGE		MSB-ONLY		NONE		
FDC/ADC REFERENCE TYPE	SINE/ARBITRARY	RAMP	CONSTANT	RAMP	ADC-SS	TDC	ADC-SS
DYNAMIC RANGE [dB]	95	92	101	127	52	143	110
FRAME RATE [fps]	30 (VARIABLE)	40	100	30	30	90	1000
EXPOSURE CODING							
CODED-EXPOSURE MODE	PER-PIXEL ARBITRARY		PER-PIXEL ARBITRARY		PER-PIXEL ARBITRARY	PER-PIXEL HDR-Only	PER 16x16 PIXELS
NUMBER OF TAPS	2	NA	2	NA	2	1	1
PIXEL CODE-RATE [Mbps]	8000		4000		850	340	69.7
SUBEXPOSURE RATE [kHz]	12500		39		23	370	1

Figure 5.8.6: Comparison of state-of-the-art image sensors with wide-dynamic-range readout and/or coded exposure.

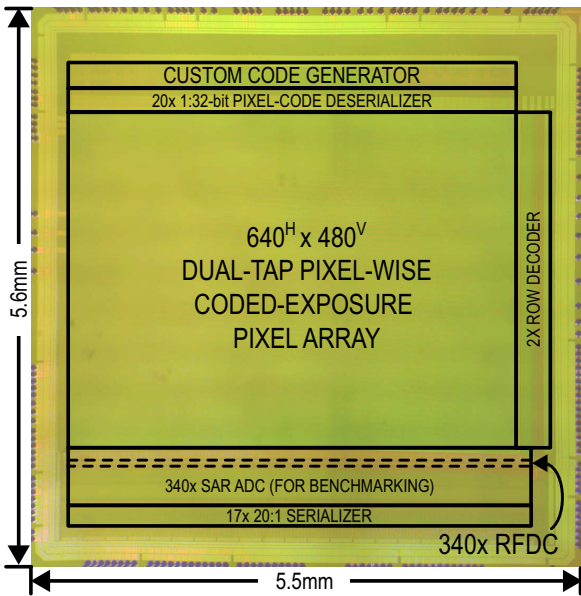


Figure 5.8.7: Micrograph of the 110nm CIS IC.